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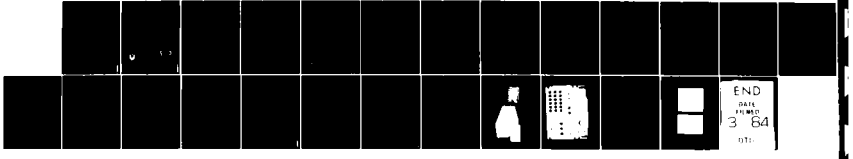

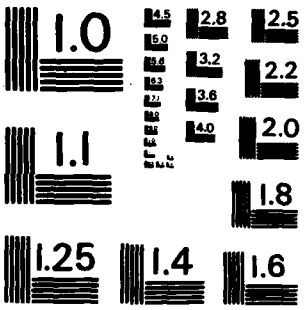

AVRADCOM

Technical Report-83-E-15

A DUAL DIGITAL TO VIDEO CONVERTER FOR AVIONICS SYMBOLOGY AND MESSAGES

VINCENT J. ORGANIC
US ARMY ELECTRONICS R&D COMMAND

EDWARD A. KARCHER
US ARMY AVIONICS R&D ACTIVITY

DECEMBER 1983

Research and Development Technical Report
Aviation Research and Development Command

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Video Display Television Display Scan Converter

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A dual digital to video converter (DVC) capable of accepting computer data, storing it in memory, and reformatting for display on a television screen is described in this report.

The converter can be used as a general purpose tool for avionics simulation work but is constructed such that it can be flown in an aircraft if desired.

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20. ABSTRACT - Continued

Two independent sets of data, such as symbology and printed messages, can be displayed simultaneously on different television monitors or combined on one monitor if desired.

The converter has its own video synchronization distribution circuitry or can be synchronized externally.

TABLE OF CONTENTS

FIGURES

LIST OF ABBREVIATIONS AND ACRONYMS

AC	Alternating Current
ATR	Airborne Transportable Receptacle
AVRADA	Avionics Research and Development Activity
CMOS	Complementary Metal Oxide Silicon
DC	Direct Current
DEC	Digital Equipment Corporation
DR-11W	Direct Memory Access Module
DVC	Digital to Video Converter
EIA	Electronic Industries Association
HORDR	Horizontal Drive (TTL for Internal Use)
NMOS	N-Channel Metal Oxide Silicon
RAMS	Random Access Memories
SYNCSELI	Select Internal or External Synchronization
TASS	Tactical Avionics Simulation Facility
TTL	Transistor Transistor Logic
TV	Television
VAX	Virtual Address Extension (DEC Trademark)
VERDR	Vertical Drive (TTL for Internal Use)

1. INTRODUCTION

This technical report describes a dual digital to video converter (DVC) capable of accepting computer data, storing it in memory, and reformatting it for display on a television screen. The converter can be used as a general purpose tool for avionics simulation work but is constructed such that it can be flown in an aircraft, if desired. Two independent sets of data, such as symbology and printed messages, can be displayed simultaneously on different television monitors or combined on one monitor, if desired. The converter has its own video synchronization distribution circuitry or can be synchronized externally.

2. SYSTEM DESCRIPTION

A typical system simulation configuration is shown in Figure 1. The VAX computer controls the operation of the DVC, cultural data generator, and map generator. The color video insetter combines three sets of outputs and provides color video drive signals to the color television monitors and the color video recording equipment.

The DVC serves to provide symbology data which is converted to a single color (of user choice) in the insetter. It also can provide paging or status messages that can be displayed directly on a small black and white television monitor. Variations of the system configuration are possible by appropriately patching the input and output video lines.

An airborne version of this system can provide the pilot and copilot with the necessary information to fly the aircraft from the television monitors, thereby reducing the pilots' workload.

3. REQUIREMENTS

a. The DVC shall have two sets of ping-pong memories, each having independent data and display capabilities.

b. The DVC shall interface with a DEC DR-11W type interface card as part of the DEC Unibus system. It shall also interface with a Singer SKC 2000 computer system. This is to be accomplished by utilizing interchangeable interface boards in the DVC.

c. The two independent display outputs shall each have a video output for directly driving a monochromatic TV monitor, and a TTL output for insetting into another external video background.

d. The displayed area shall have a square format with a resolution of 256 bits per displayed line.

e. The DVC shall incorporate a built-in TV synchronization generator, and be capable of being synchronized from an external source.

f. DVC construction shall be of airborne quality, powered by a 28-volt DC power supply to permit installation on aircraft, if required.

4. DESCRIPTION OF THE DIGITAL TO VIDEO CONVERTER

Figure 2 is a block diagram of the DVC. The DVC was designed to have interchangeable computer interface boards to permit operation with either the SKC 2000 or Unibus interfaces. Data is written into the DVC via the 32-line data bus of the computer interface. The data bus can be utilized in either a 32-line single-ended configuration for the SKC 2000 interface or 16-line differential configuration for

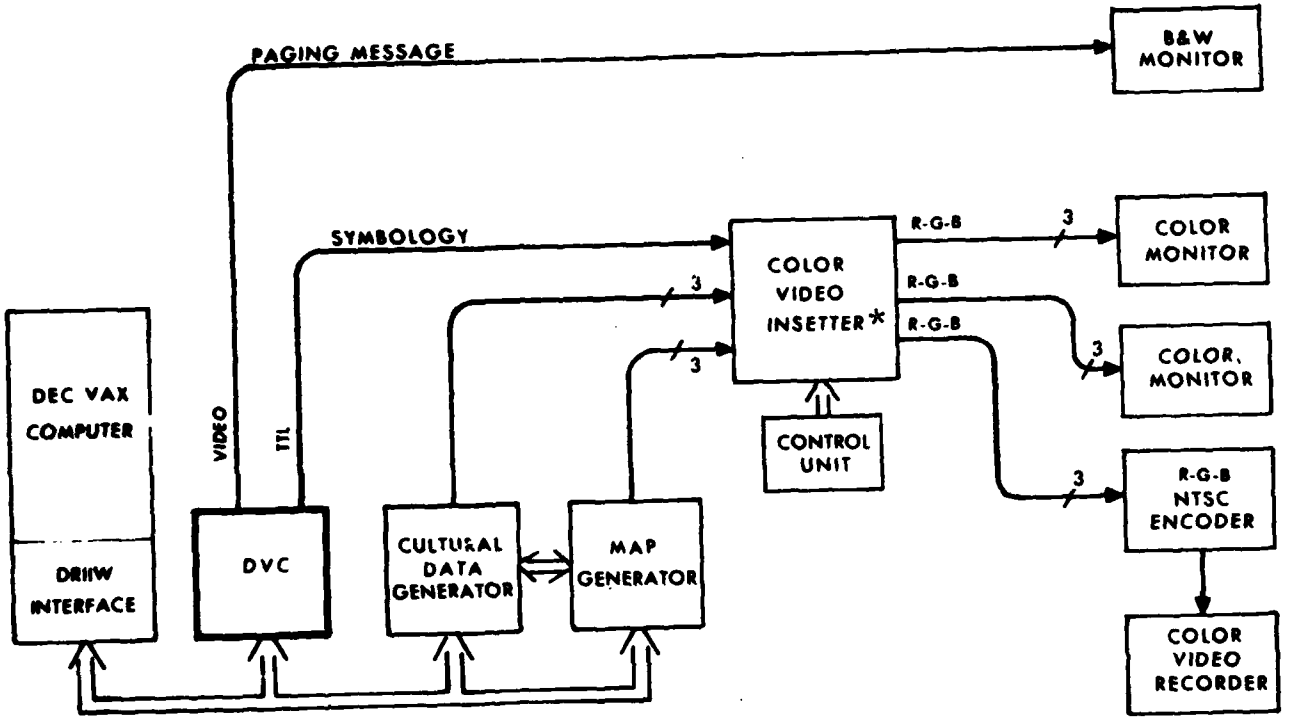


Figure 1. Block Diagram of Display System.

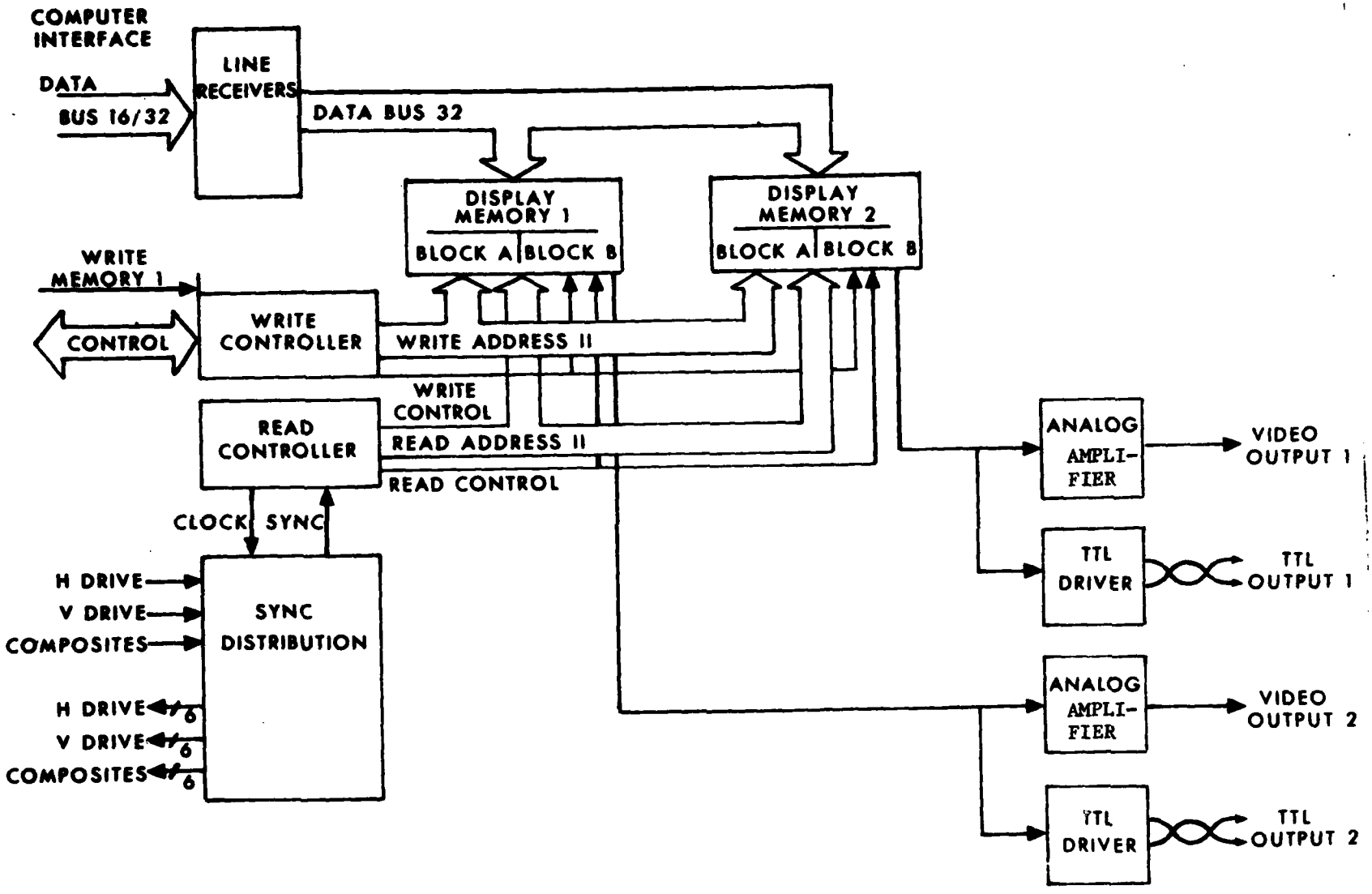


Figure 2. Block Diagram of Digital to Video Converter.

the Unibus interface. An internal data bus of 32 bits in width routes data to each Display Memory. Data is written into memory in 32-bit words for the SKC 2000 and as two 16-bit words for the Unibus. Data is transferred from the host computer in a block transfer mode. One block of data is utilized for each display frame and consists of 1840 32-bit words (230 lines by 256 pixels/line). The data is displayed in accordance with the format of Figure 3. The Write Controller supervises the data block transfer at the request of the host computer.

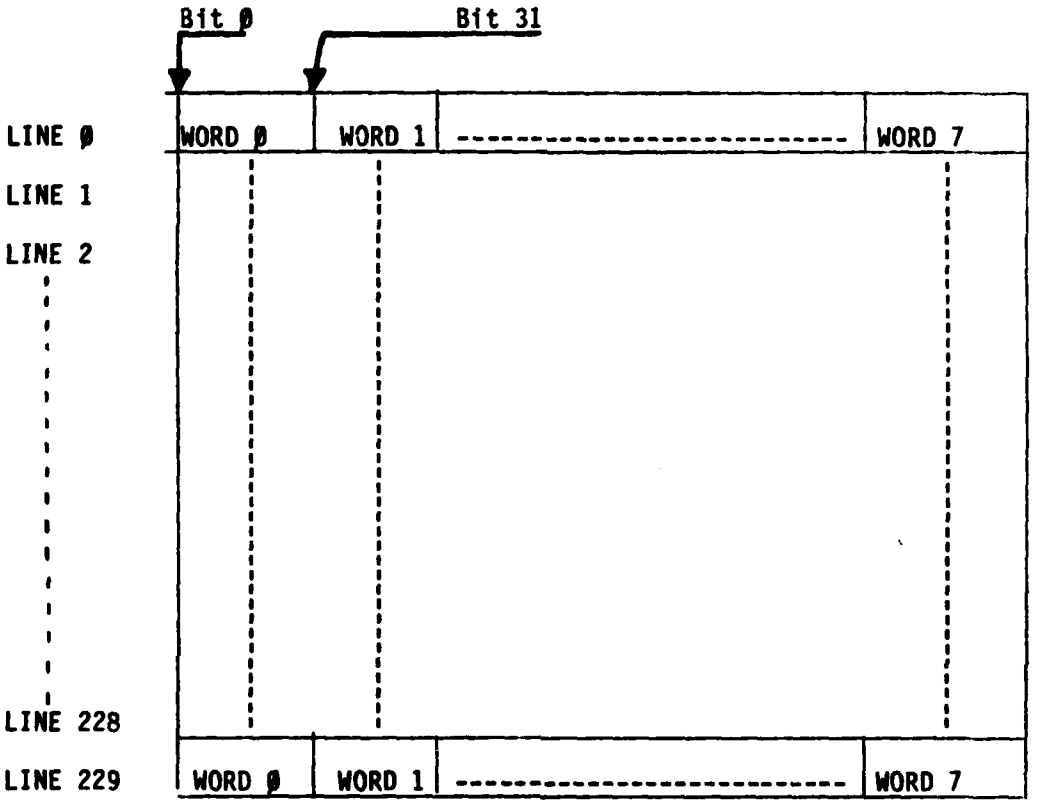
Two independent Display Memories are available to the host which directs the Write Controller via the Write Display Memory 1 control line to write data into Display Memory 1 or Display Memory 2. Each memory feeds its own video and TTL output for the driving of external television monitors and display equipment. Each Display Memory is organized as blocks A and B. Each block stores one display frame of data and is operated in a "ping-pong" manner to permit one block to be loaded by the host while the other block is being displayed. The swapping of memory blocks is performed by the Write Controller upon completion of a block transfer from the host. The display supervision of the memory blocks being displayed is performed by the Read Controller.

The Read Controller provides the memory address, controls signals, and synchronizes the data with the television synchronization signals. The Synchronization Distribution circuity provides standard television synchronization signals for use internal to the converter and distribution to external equipment. Each function in the converter is described in more detail in paragraphs a through f.

a. Computer Interfaces.

(1) SKC 2000 Computer Interface (Fig. 4). The interface receives all data and control commands from the computer and supervises the writing of data from the computer into the Display Memories. The input receivers receive data on the 32-line single-ended bus from the computer and distribute the data to the Display Memories over the internal 32-line data bus. The interface logic interfaces the control lines to the computer and front panel. The Master Clear line from the computer clears all logic circuitry within the DVC. The Manual Clear line clears the DVC logic circuitry from a push button located on the front panel. The Write Memory 1 line is used by the computer to specify the Display Memory which shall receive the transferred data. This line is run to the write controller and activates the applicable bus enable lines for the respective Display Memories 1 and 2. A logic 1 is for Display Memory 1 and a logic 0 is for Display Memory 2.

The DVC places a logic 1 on the Data Request line to signal the computer that a word can be transferred to the DVC. The computer responds by placing a logic 1 on the Data Available line when the word to be transferred is ready on the data bus and, upon receipt, the DVC returns the Data Request line to a logic 0. The DVC responds by placing a logic 1 on the Data Acknowledge line when the data has been written into the Display Memory. A short time later the DVC places a logic 1 on the Data Request line to request the next word transfer. For each word transferred, a memory write strobe is generated for Display Memory 1 or 2 and the address counter is advanced one state. The address is then placed on the write address bus. The address counter starting state is determined by the start address select switch. The Write Controller operates in a block transfer mode. An 1840-word block is accepted from the computer and written into the selected Display Memory as block A or B. The block has sufficient storage for one display frame. At the end of the block transfer, the Write Controller interchanges the memory blocks so that the block with the most recent data is placed in the read mode and the alternate block made available to the host computer for update.



NOTE: Shown for SKC 2000 - 32 Bit Format

For UNIBUS 16 Bit Format:

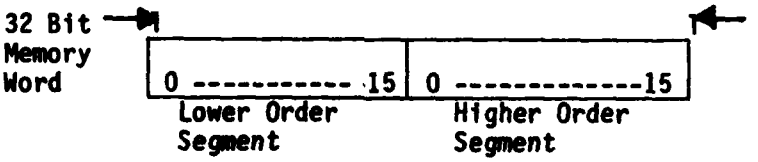


Figure 3. Display Format.

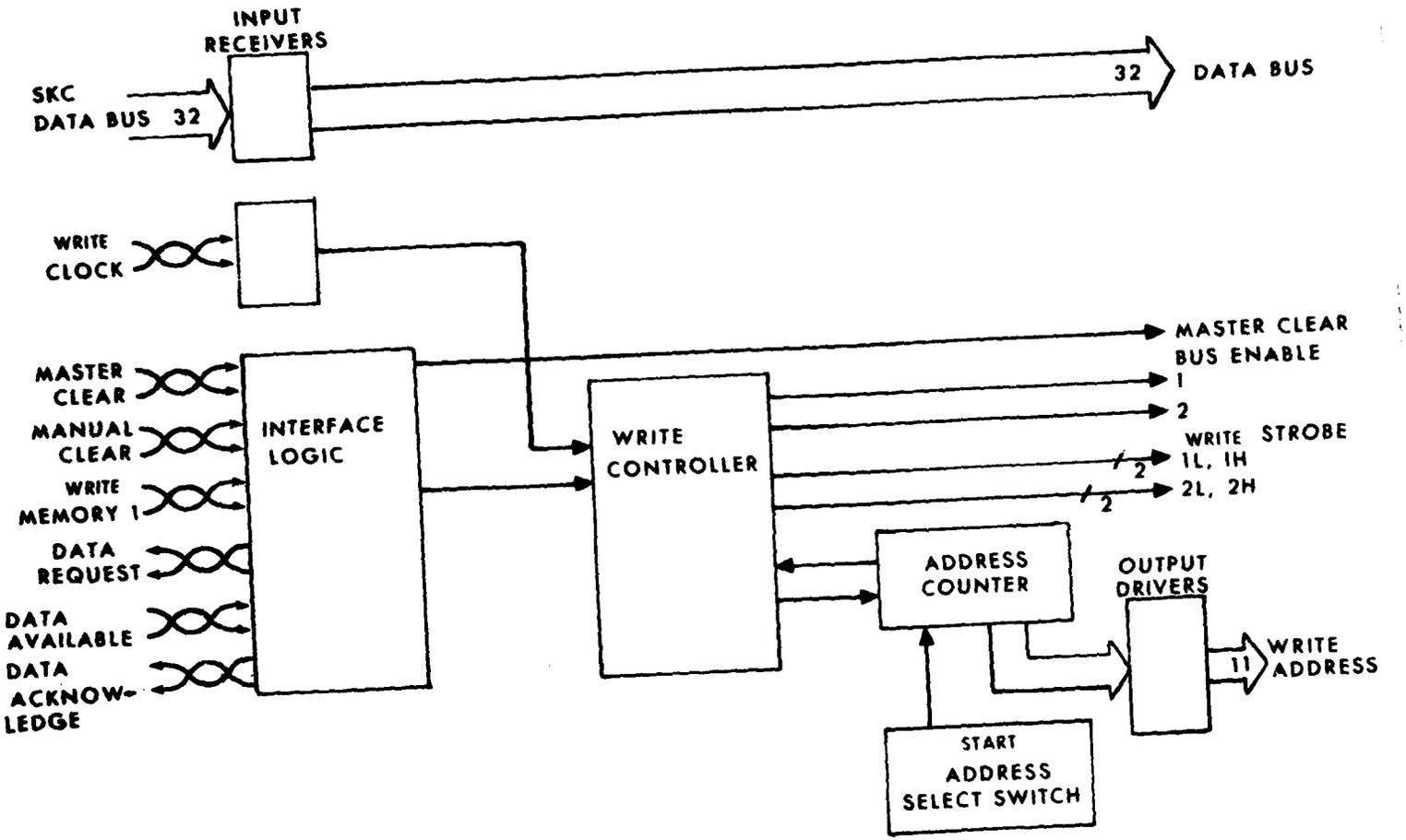


Figure 4. SKC 2000 Computer Interface.

(2) Unibus Interface (Fig. 5). The Unibus Interface is similar to the SKC 2000 Interface with the exception of the data bus and interface control signals. The data bus from the computer is 16 lines in width and utilizes the long lines drivers for differential TTL signals being transmitted over twisted wire pairs per data line. Within the DVC, the input receivers convert the differential TTL to a single-ended format. The 32-line data bus to the Display Memories is formed by connecting the 16 lines from the computer directly to lines 0-15 (lower order segment) of the bus and also to lines 16-31 (higher order segment), respectively. Each Display Memory is organized into lower and higher order segments which can be written into by separate write strobes from the display controller. Thus, two 16-bit word transfers are required from the host computer to fill one 32-bit display word storage location to memory. There is also a difference in the control interface signals. The Master Clear, Manual Clear, and Write Memory 1 lines function in the same manner as the SKC 2000 Interface. Concerning the balance of the control lines, the host computer places a logic 1 on the Go 1 line to request a block transfer be made to the DVC. The DVC responds by placing a Logic 1 on the Cycle Request line to the host. When the host has a data word ready for transfer, it places a logic 1 on the End Cycle line to the DVC. The DVC lowers the Cycle Request line and writes the word into Display Memory. When the write cycle is complete, the DVC places a logic 1 on the Cycle request line indicating that the next word transfer can take place. Word transfers continue to take place from the host until the entire block transfer is complete.

b. Display Memories. Figure 6 is a block diagram of a Display Memory. Two independent Display Memories (1 and 2) are used in the DVC. Each Display Memory is, in turn, divided into two blocks (A and B), 2K words deep by 32 bits wide. Each block contains sufficient storage for one frame of data, 1840 words by 32 bits wide. Four MK4802-3 2K by 8-bit static N-channel metal oxide silicon (NMOS) random access memories (RAMS) manufactured by Mostek are used for each memory block. Complementary metal oxide silicon (CMOS) RAMS such as the RCA CDM6116 with the same organization could also be directly substituted with a resulting lower power consumption. The data display format is shown in Figure 3. Control signals which determine the operating mode of the memory come from the Write Controller. The Write Controller operates the memory blocks in a "ping-pong" mode; i.e., one block being displayed while the other block is available to the host computer for update. To write data into a memory block, data enters via the data bus and is routed to the desired block by the data switch. Similarly, the write address is routed to the memory block through the address multiplexer. A write strobe is supplied by the Write Controller. To read a memory block, data flows from the memory through the data multiplexer to the parallel-to-serial converter. The Read Controller supplies the read address which is routed to the memory through the address multiplexer and also controls the operation of the parallel-to-serial converter. The serial output data is fed to two output drivers: a differential logic driver for routing of the data to the Video Output board, and a TTL differential driver for output of the data to the DVC front panel for use by external display equipment.

c. Read Controller (Fig. 7). The Read Controller supervises the access of data from the Display Memories, conversion of the data to a serial format, and synchronization of the displayed data with the television synchronization signals. A 27.72-MHz oscillator serves as the source of the master clock for the DVC. All clock, other clock, read clock, write clock, and synchronization distribution clock signals, are derived from this source. The horizontal and vertical drive signals synchronize the Read Controller to the television sync signals. When vertical drive arrives, the vertical position counter is started and counts the number of raster lines skipped until the start of the displayed active video. The number of lines skipped is determined by the setting of the vertical position switch. When the proper scan line has arrived to start the active video, the horizontal position counter then initiates the active video in the desired location on each raster scan line by counting pixel spaces to be skipped from the receipt of the horizontal drive pulse for each line. The

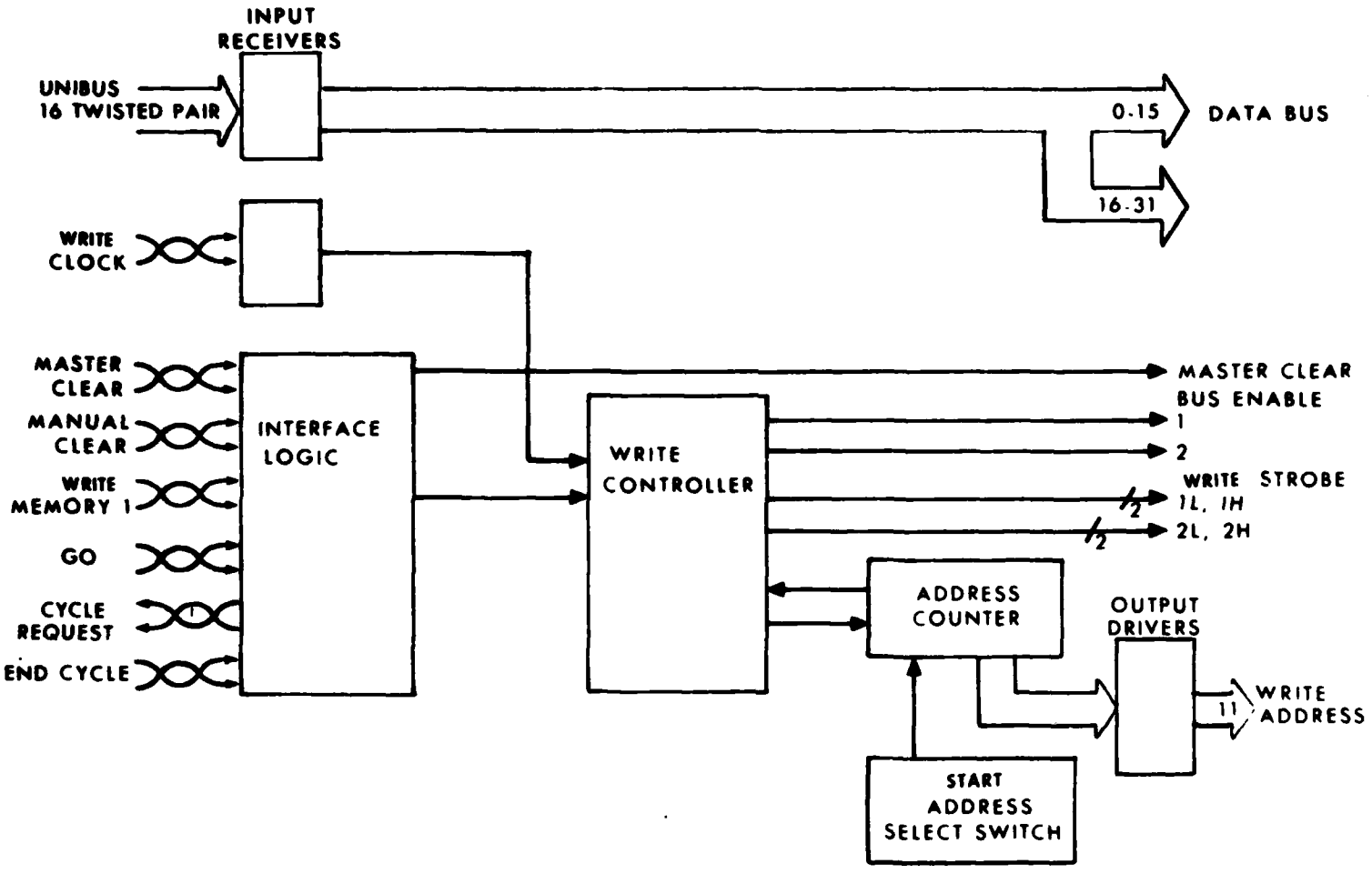


Figure 5. Unibus Interface.

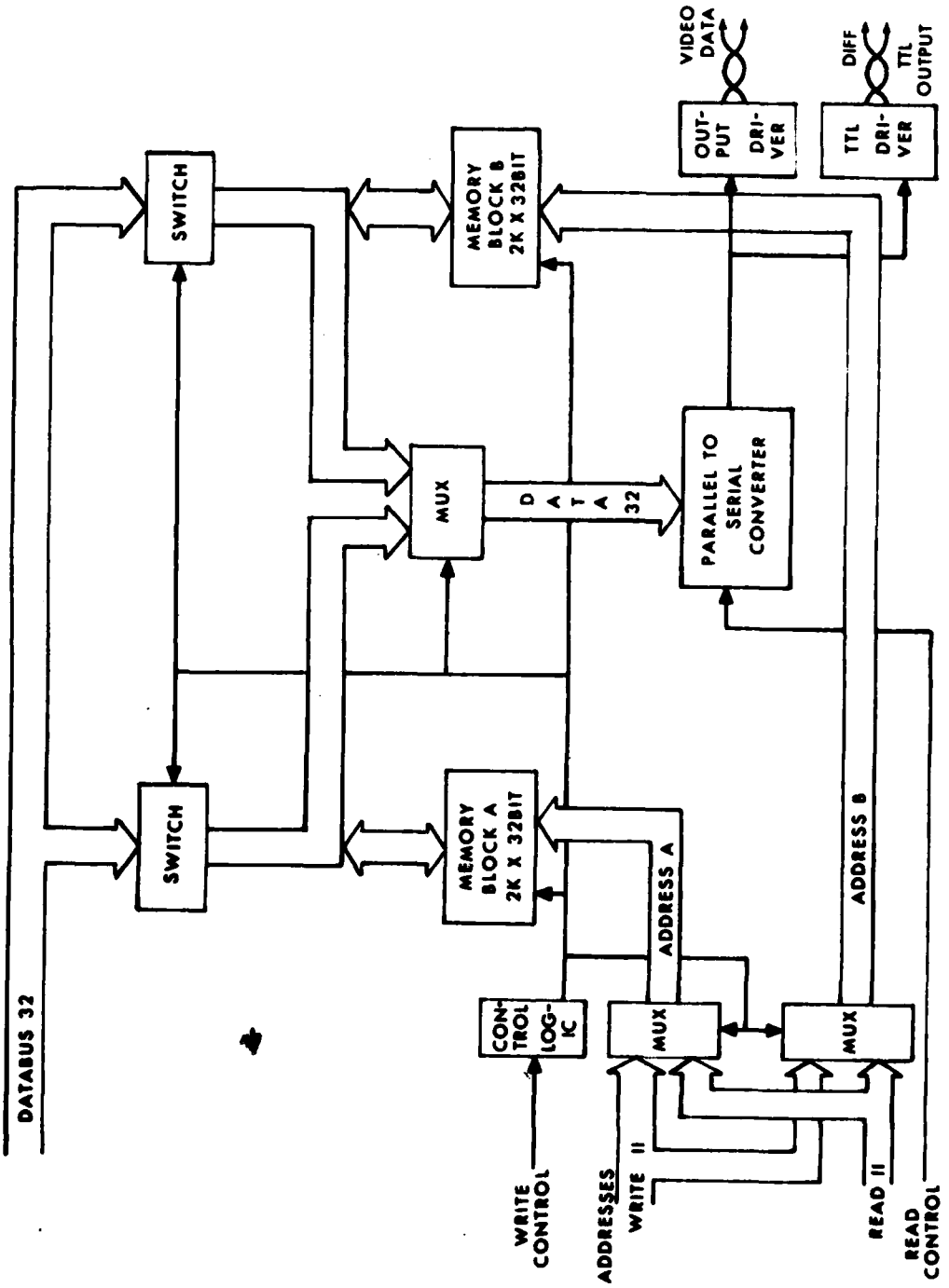


Figure 6. Display Memories.

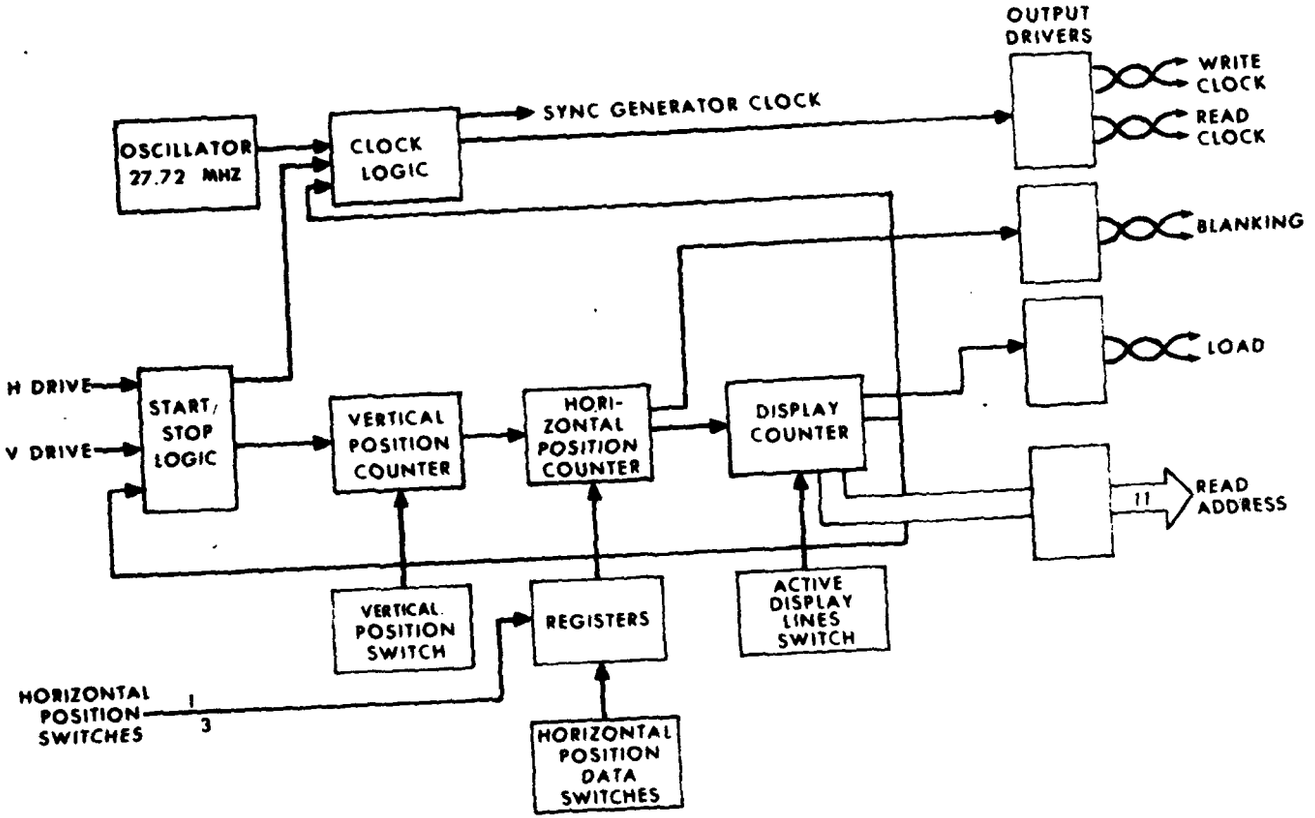


Figure 7. Read Controller.

starting count (horizontal position) is determined by the horizontal position word stored in the register. The horizontal position switch on the front panel selects the starting position (left, center, right) by selecting the proper position starting data stored in the position data switches. Once the active video has started, the display counter is enabled and furnishes the required read addresses to the Display Memories. The number of active raster display lines is determined by the setting of the display lines switch. When the entire frame of data has been read from the Display Memory, the display counter overflows and places the Read Controller in an idle state until the next vertical drive pulse arrives to initiate a new read cycle. The read clock, blanking, and load commands are routed to the Display Memory cards for operation of the parallel-to-serial converters.

d. Video Output (Fig. 8). Data is received by the line receivers from each respective Display Memory on twisted pair differential logic lines. The line receiver output is then scaled to the desired 0-to-1-volt video level and fed to output amplifiers for driving the 75-ohm input impedance of the two television monitors.

e. Synchronization Distribution (Fig. 9). This board provides synchronization for internal circuitry as well as furnishing television synchronization signals for distribution for up to six external video users. The board has its own sync generator for use when the converter is the master sync distribution center for the display system. The clock signal for the sync generator is derived from the converter master clock to maintain synchronization with the rest of the converter functions. Synchronization signals can also be provided from an external master source. External sync signals at either the standard EIA or TTL levels are possible depending upon the setting of the sync level multiplexer. This setting is hardwired at the board level to accept the EIA level. A control signal, SYNCSELI, is connected to the sync select switch on the front panel and switches the output multiplexer between internal or external sync signals to permit control of the sync source. The upper set of output drivers provide synchronization (HORDR, VERDR), at TTL levels to other sections of the converter. The output level shifters shift the level of the sync signals to EIA levels and provide six 75-ohm drivers for each signal (i.e., horizontal drive, vertical drive, and composite sync for external distribution).

f. Power Supply (Fig. 10). The Power Supply supplies all necessary operating potentials required for operation of the converter circuitry. The supply is modular in construction consisting of a number of power modules manufactured by Power Cube Corporation. The prime power input to the Power Supply is 28 volts DC from the aircraft power system which feeds an AC converter module. The output from the AC converter feeds the power converter modules which furnish the output DC potentials. All modules are mounted in an enclosure and all input and output potentials are routed into the enclosure through EMI filters. The enclosure is mounted on a heat sink located on the back of the converter ATR box. The power distribution within the converter is via a power bus and appropriate cabling. The total power input to the converter is 1.8 amperes at 28 volts DC.

5. FABRICATION

A total of six circuit boards, 17.5 by 25 cm (7 by 10 inches), were required and are housed in a commercially available ATR airborne enclosure (Fig. 11). The digital circuitry was mounted on wire wrap boards. Analog circuitry was mounted on two custom printed circuit boards. Figure 11 shows typical circuit boards from the converter. Commercially available linear and digital integrated circuits were used in each circuit board assembly. The front panel (Fig. 12) contains all input/output, power, and electrical voltage test points.

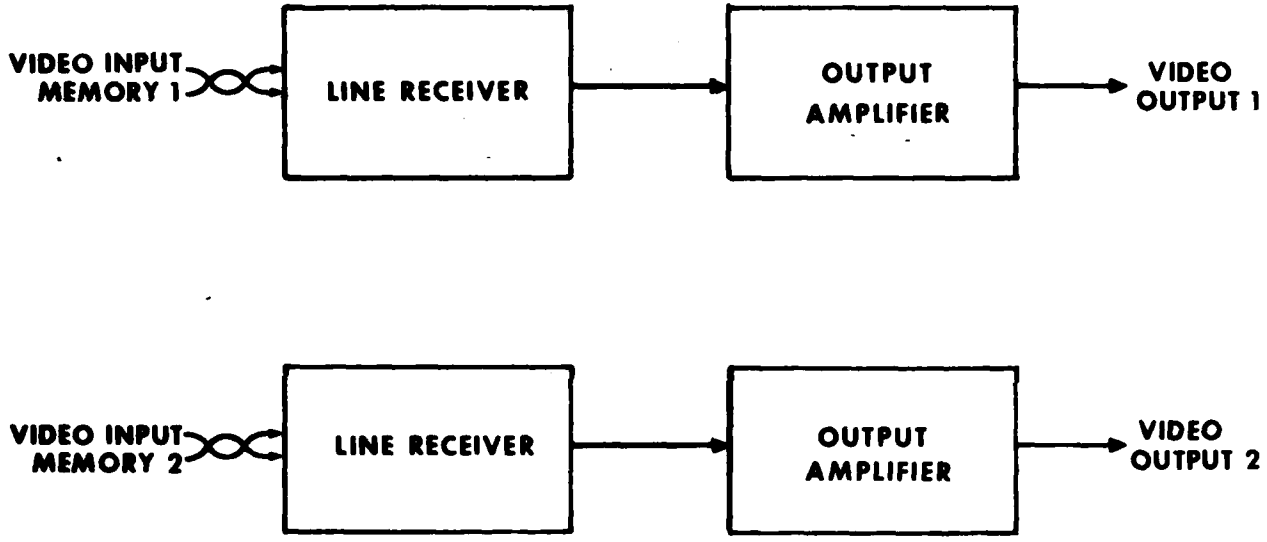


Figure 8. Video Output.

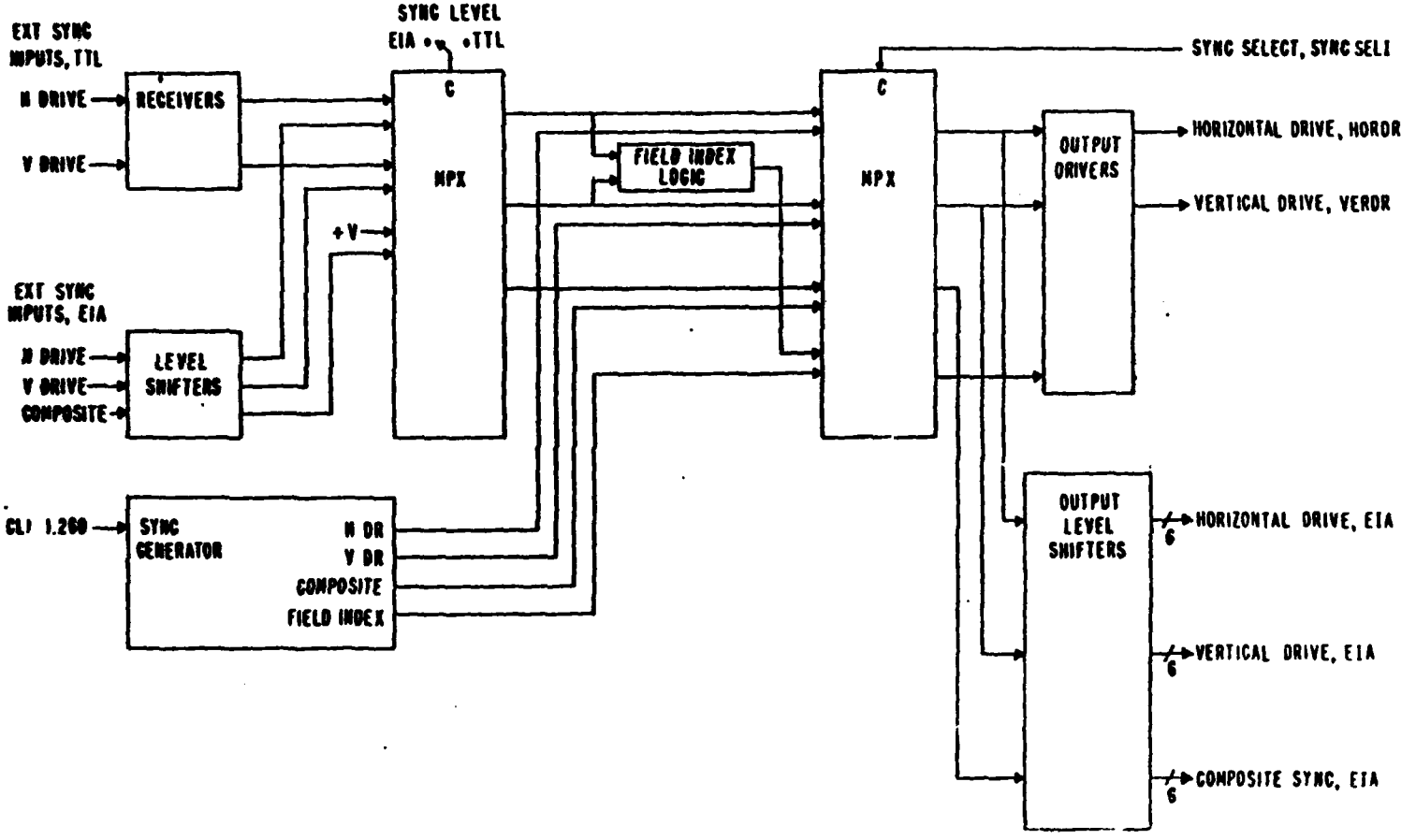


Figure 9. Synchronization Distribution.

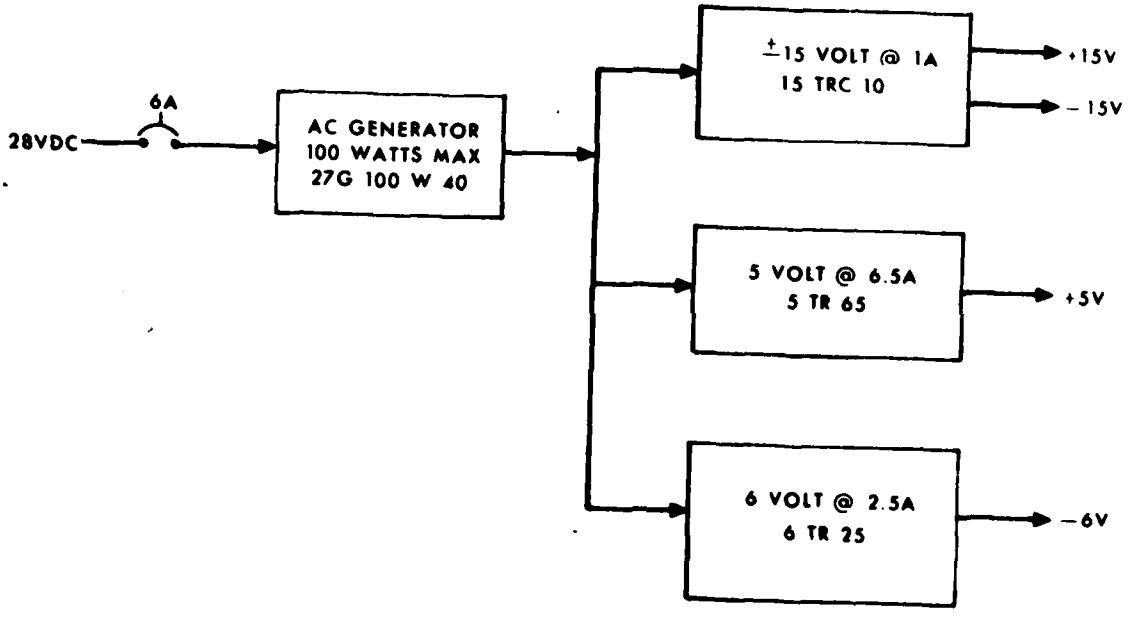


Figure 10. Power Supply.

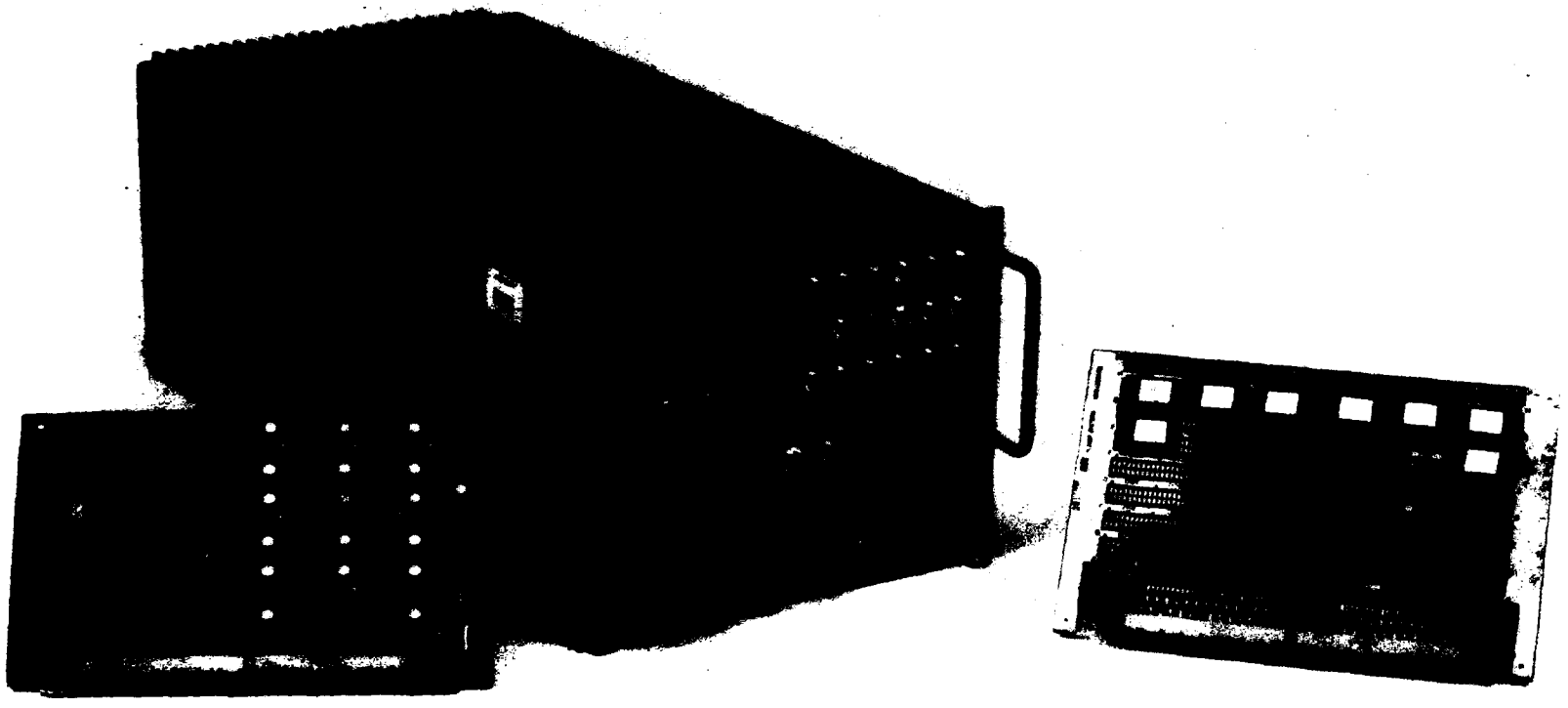


Figure 11. Digital to Video Converter and Typical Circuit Cards.

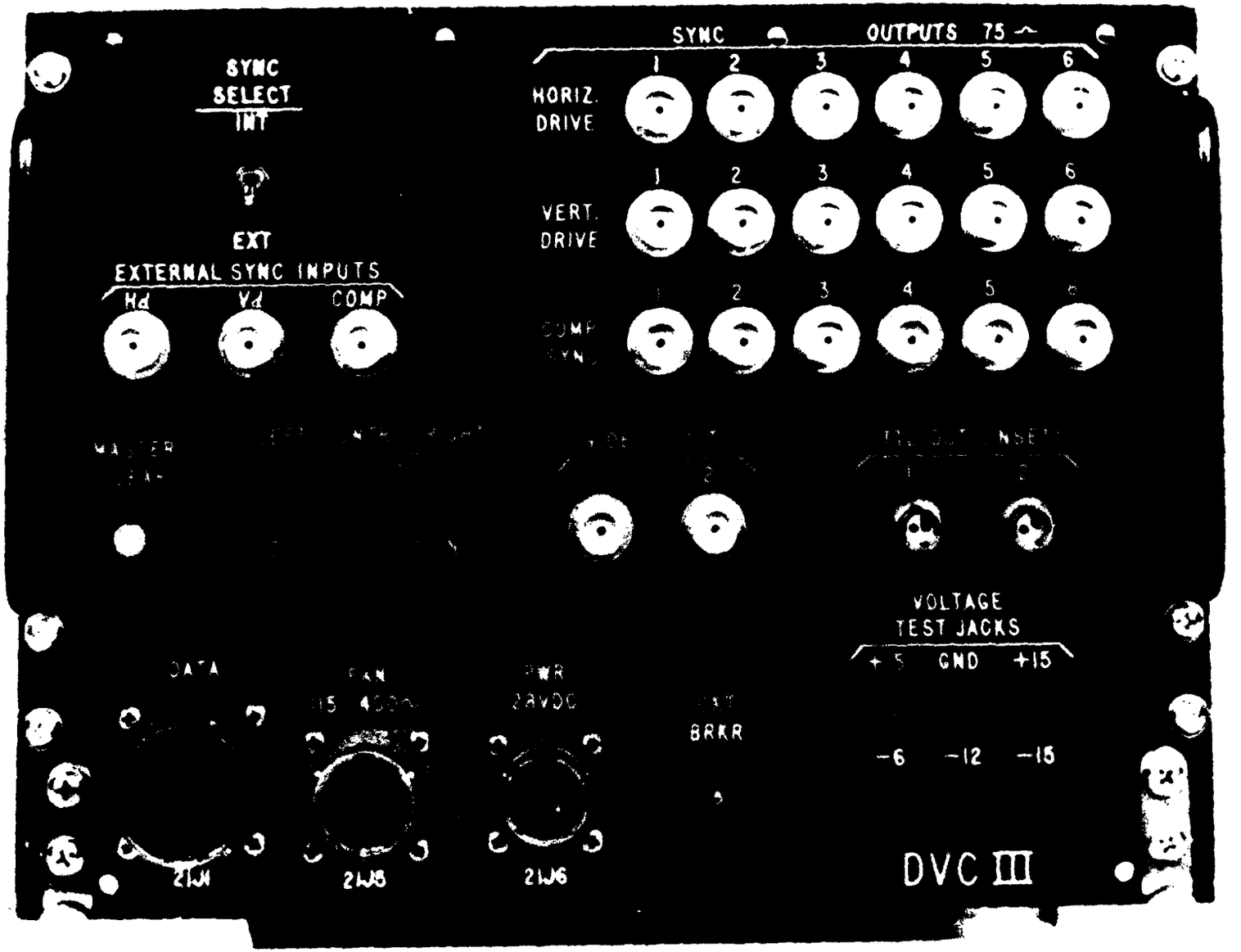


Figure 12. Digital to Video Converter Front Panel.

6. TEST RESULTS

The DVC has been tested successfully and is operating in the Tactical Avionics System Simulation Facility of AVRADA. Figure 13 depicts some typical avionic display formats that are used in both simulation and aircraft.

7. CONCLUSIONS

A general purpose Digital to Video Converter which is capable of airborne operation has been designed and fabricated. The converter has dual Display Memories and has been hosted from both an SKC 2000 and a Unibus interface. The converter has been successfully operated in the laboratory with computer-generated symbology and alphanumeric messages, and has met all design goals. The extensive use of modern microelectronic circuitry has made feasible the fabrication of the converter and its packaging into an airborne enclosure.

ACKNOWLEDGMENTS

The authors wish to acknowledge the contributions of Mr. J. VanDover and Mr. B. Turner of the Electronics Technology and Devices Laboratory and Technical Support Activity, respectively, of ERADCOM for their assistance in the fabrication of circuit boards and assembly of the converter, and Mr. R. Kelly of Vitronics for generation of the software used in debugging the converter.

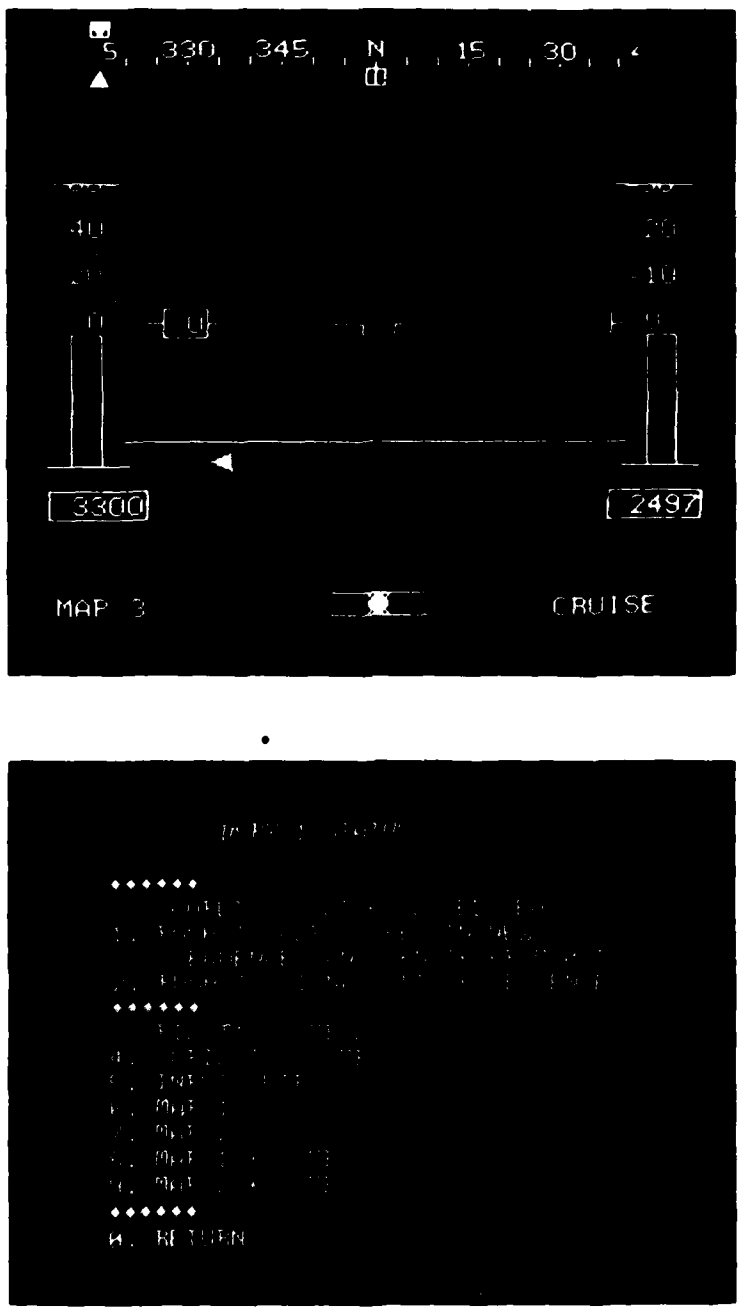
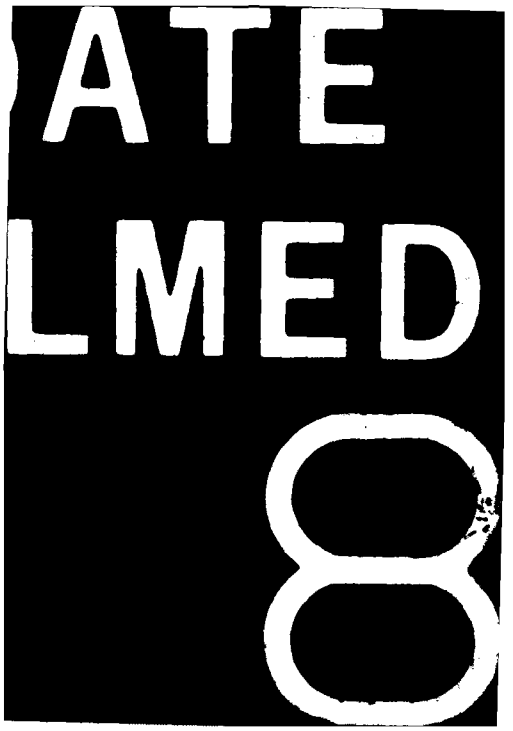


Figure 13. Typical Avionics Displays.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